

1   **ABSTRACT**

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3   A software programmable DSP with a field programmable instruction set is described  
4   where customized instructions can be created, or certain existing instructions can be  
5   modified, at the user's location after taking delivery of the processor. The FPGA fabric  
6   used to implement the reprogrammable instructions is restricted to supporting the  
7   software-programmable DSP - never functioning as an independent coprocessor - and  
8   therefore enabling the reprogrammable instructions to exist in the normal stream of DSP  
9   software execution. DSP-type functions implemented in the FPGA fabric are also  
10   restricted to being automatically generated such that they are synchronous with the  
11   processor clocks - enabling easy conversion to an ASIC. Designs implemented on a die  
12   containing a DSP with an FPGA-style reprogrammable instruction fabric may be  
13   migrated to a smaller die within a family of DSP die containing hard-wired ASIC  
14   instruction fabrics, all members of this ASIC family having common I/O functionality to  
15   enable operation in the same system socket.

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